OIPE IAP23
APR 25 2006
PATENT & TRADEMARK OFFICE

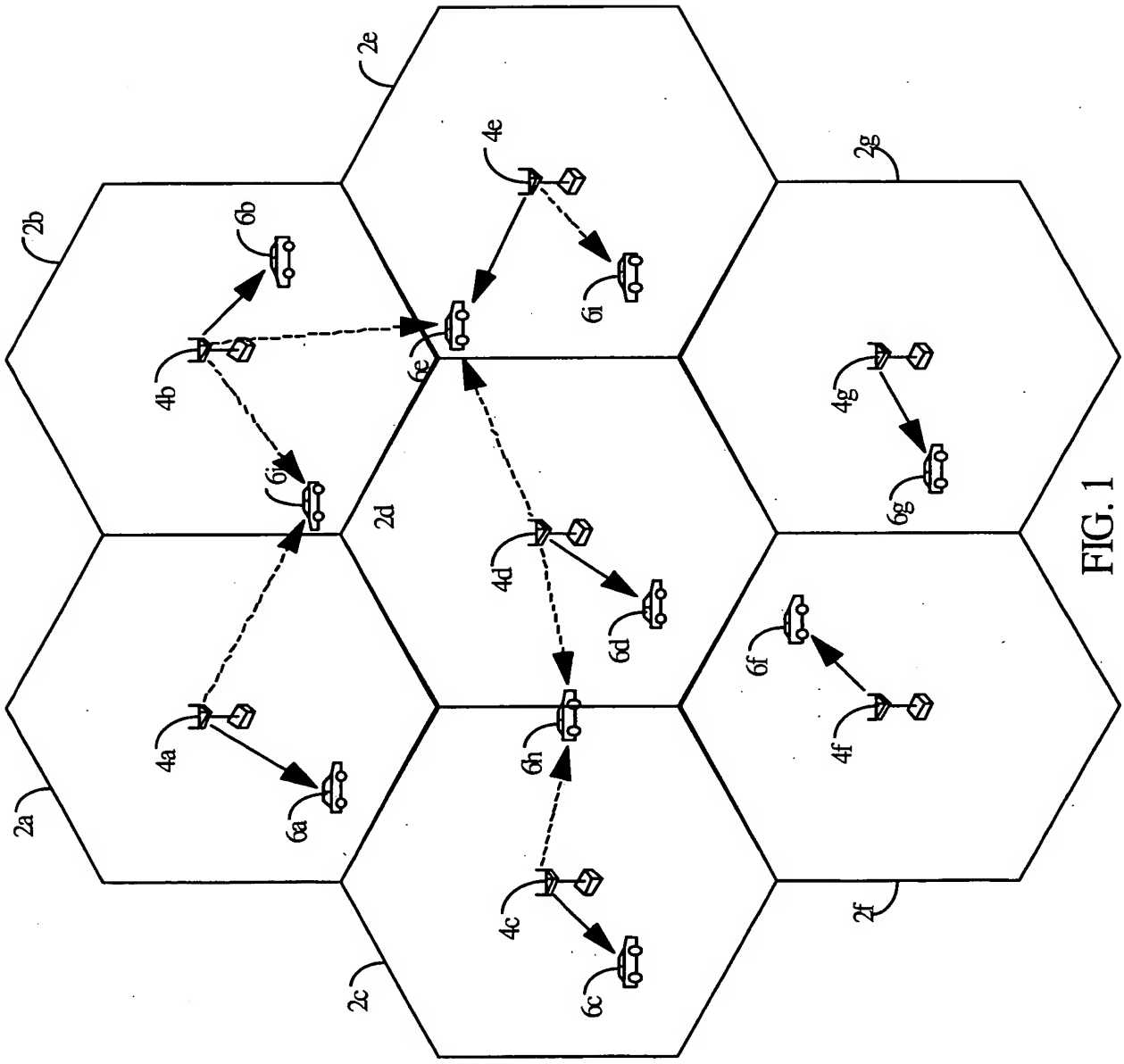

FIG. 1

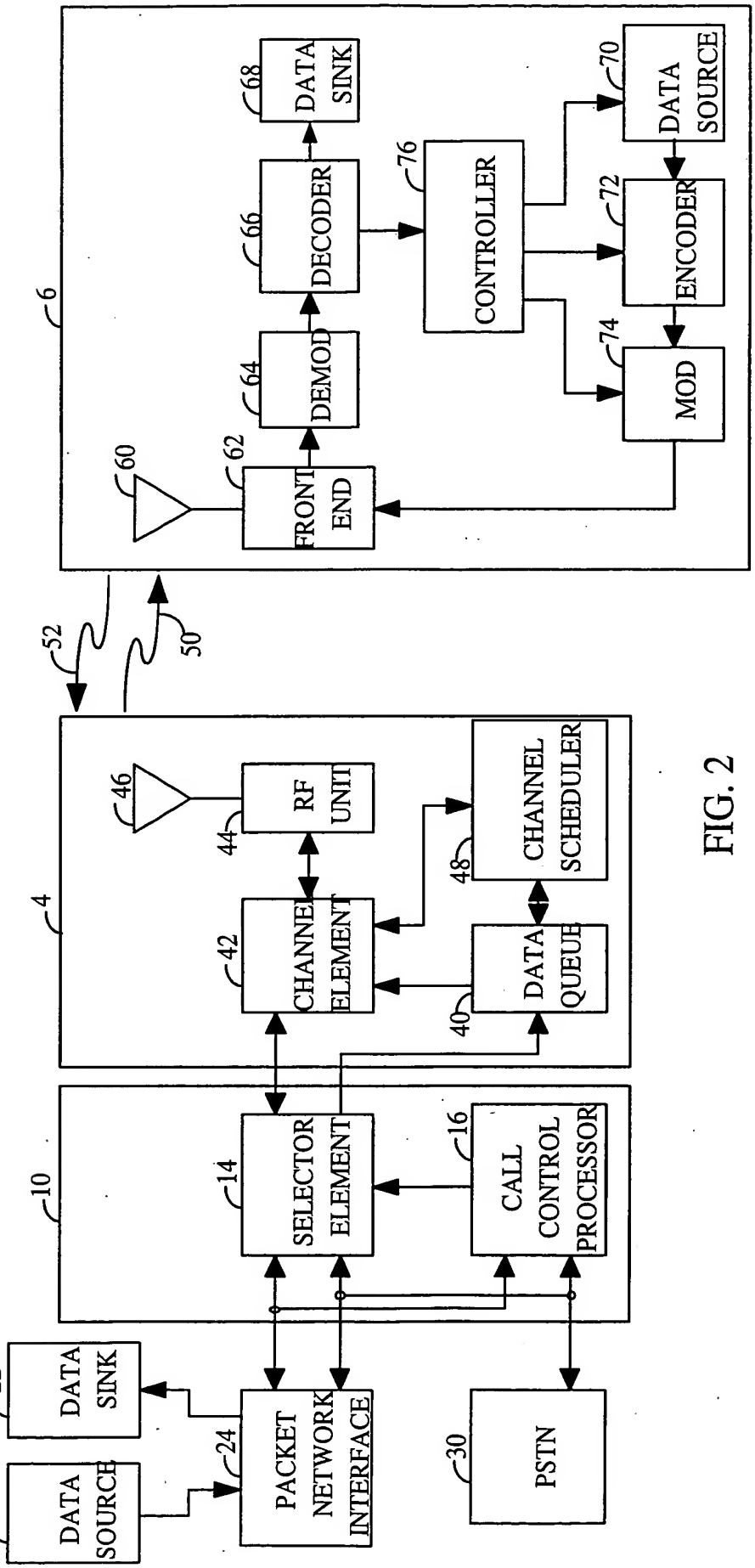
DATA SOURCE
20
DATA SINK
22
PACKET NETWORK INTERFACE
24
PSTN
30
10
SELECTOR ELEMENT
14
CALL CONTROL PROCESSOR
16
4
RF UNIT
44
46
CHANNEL ELEMENT
42
CHANNEL SCHEDULER
48
DATA QUEUE
40
52
50
6
FRONT END
62
60
DEMOD
64
DECODER
66
DATA SINK
68
CONTROLLER
76
MOD
74
ENCODER
72
DATA SOURCE
70

FIG. 2

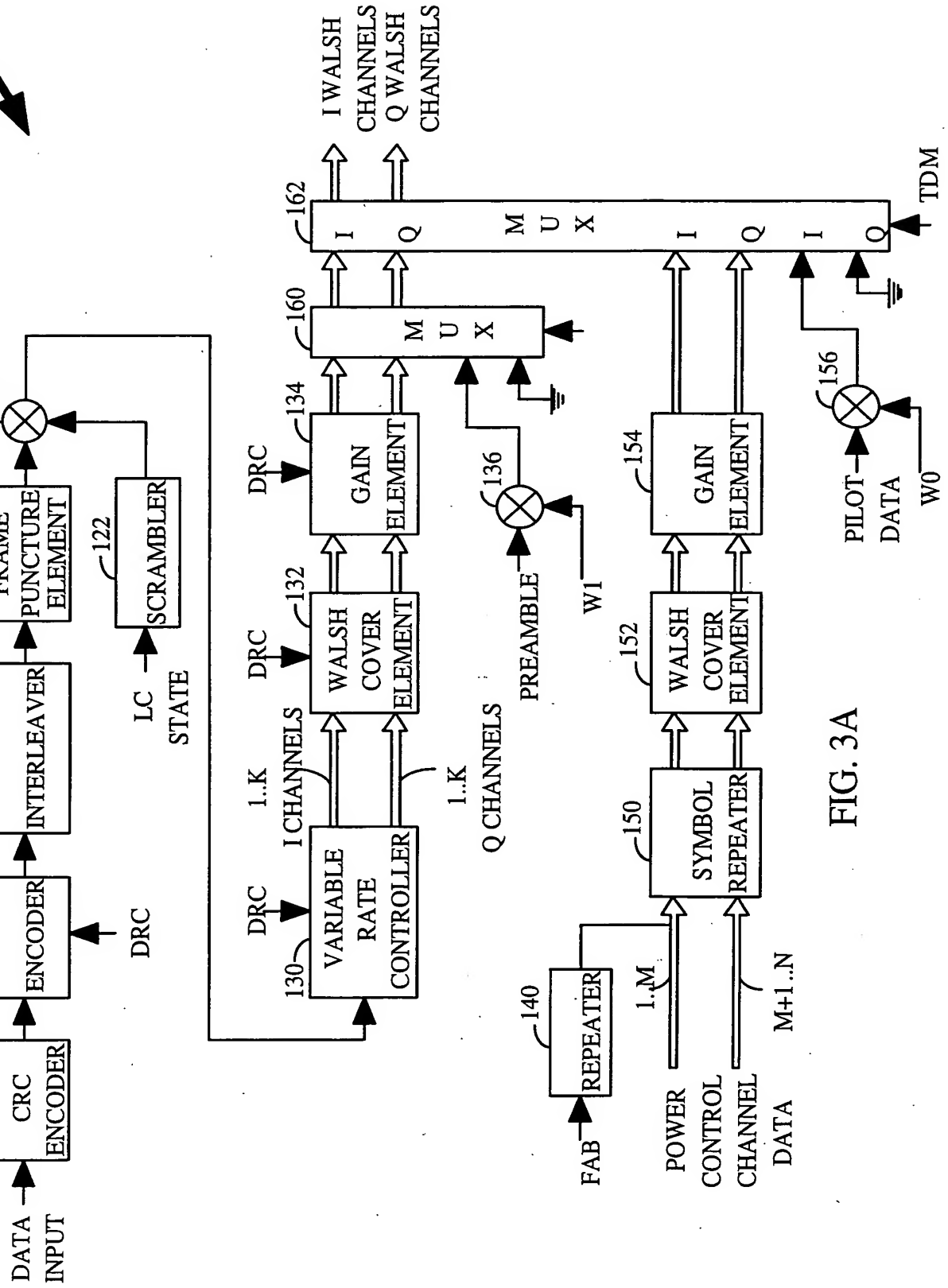
42
DATA INPUT
112
CRC ENCODER
114
ENCODER
DRC
116
INTERLEAVER
118
FRAME PUNCTURE ELEMENT
120
LC STATE
122
SCRAMBLER
DRC
130
VARIABLE RATE CONTROLLER
1..K I CHANNELS
1..K Q CHANNELS
DRC
132
WALSH COVER ELEMENT
DRC
134
GAIN ELEMENT
136
PREAMBLE
W1
160
M U X
162
M U X
I WALSH CHANNELS
Q WALSH CHANNELS
TDM
140
REPEATER
FAB
1..M
POWER CONTROL
M+1..N
CHANNEL DATA
150
SYMBOL REPEATER
152
WALSH COVER ELEMENT
154
GAIN ELEMENT
156
PILOT DATA
W0

FIG. 3A

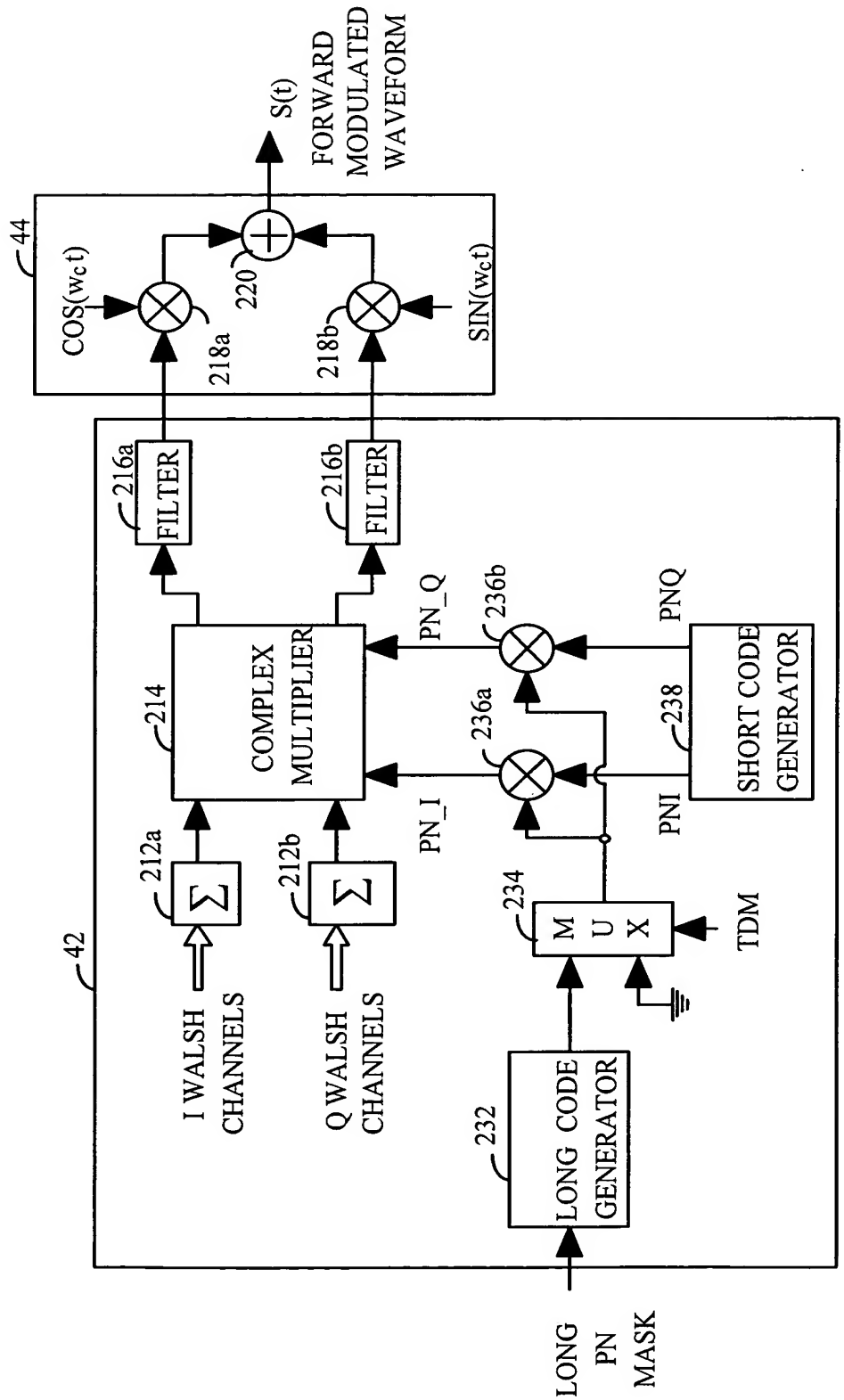
S(t)
FORWARD
MODULATED
WAVEFORM
44
COS(wc t)
220
SIN(wc t)
218a
218b
216a
FILTER
216b
FILTER
42
214
COMPLEX
MULTIPLIER
PN_Q
236b
PNQ
236a
238
SHORT CODE
GENERATOR
PN_I
PNI
212a
212b
234
M
U
X
TDM
I WALSH
CHANNELS
Q WALSH
CHANNELS
232
LONG CODE
GENERATOR
LONG
PN
MASK

FIG. 3B

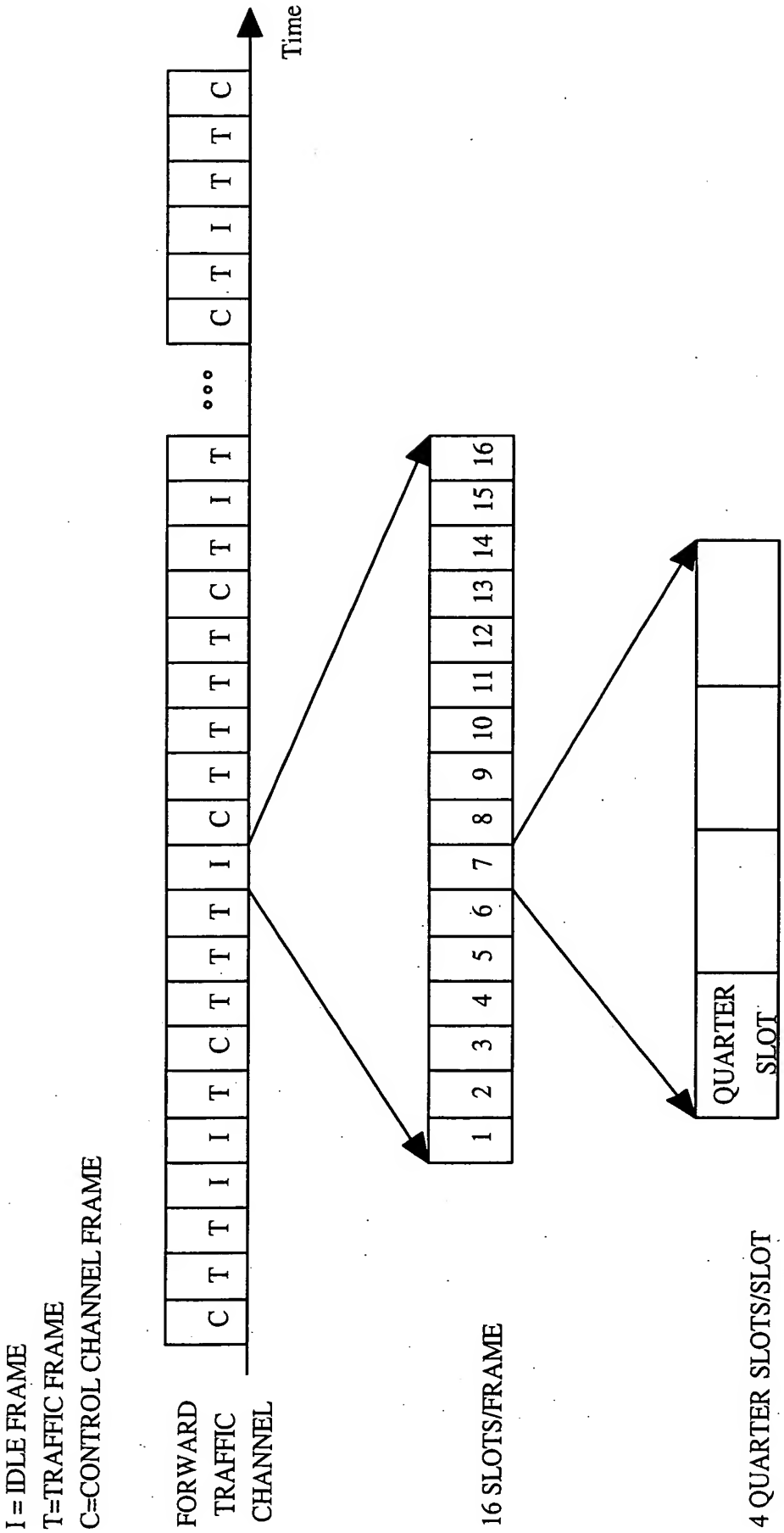
I = IDLE FRAME
T=TRAFFIC FRAME
C=CONTROL CHANNEL FRAME
FORWARD TRAFFIC CHANNEL
Time
C T T I I I T C T T I C T T T T C T I T ... C T I T T T C
16 SLOTS/FRAME
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
4 QUARTER SLOTS/SLOT
QUARTER SLOT

FIG. 4A

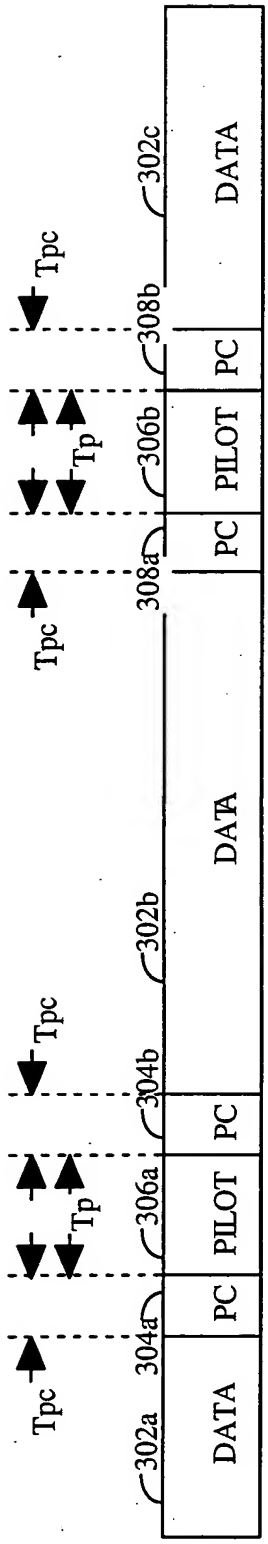
1 SLOT
DATA
PC
PILOT
PC
DATA
PC
PILOT
PC
DATA
302a
304a
306a
304b
302b
308a
306b
308b
302c
Tpc
Tp
FORWARD TRAFFIC CHANNEL
POWER CONTROL CHANNEL
PILOT CHANNEL

FIG. 4B

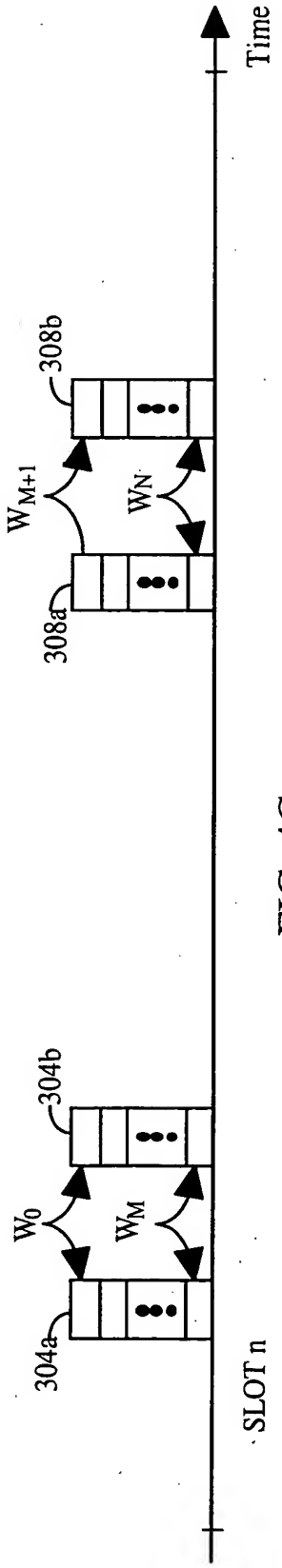
Time
SLOT n
304a
304b
308a
308b
W0
WM
WM+1
WN
POWER CONTROL CHANNEL

FIG. 4C

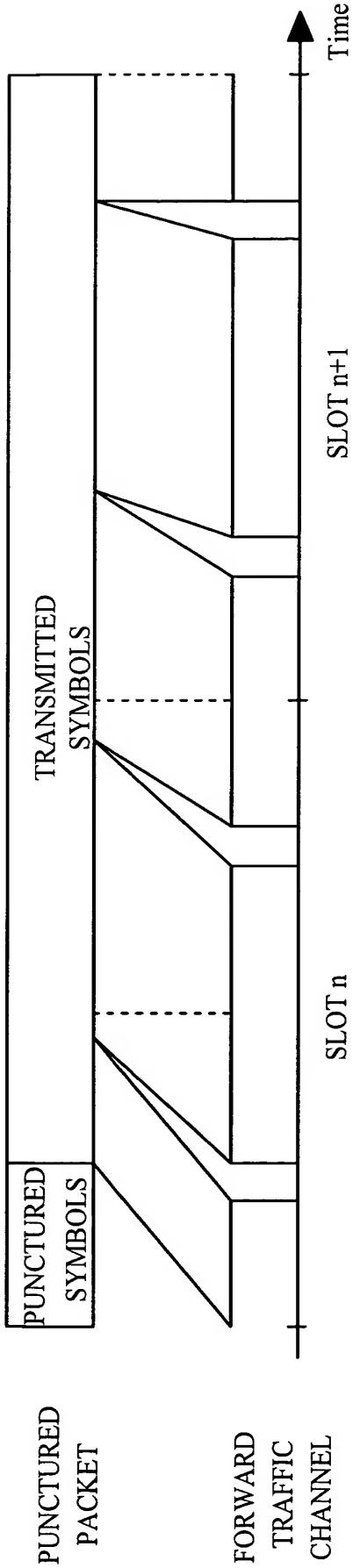
Time
SLOT n+1
SLOT n
TRANSMITTED SYMBOLS
PUNCTURED SYMBOLS
PUNCTURED PACKET
FORWARD TRAFFIC CHANNEL

FIG. 4D

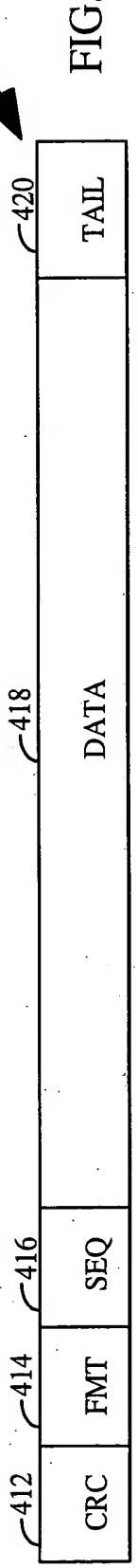

FIG. 4E

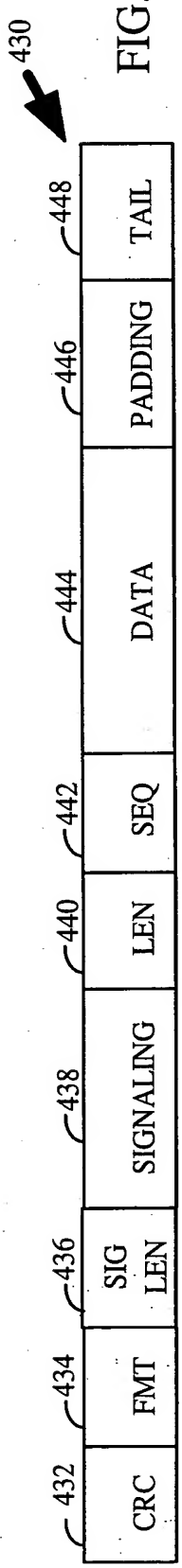

FIG. 4F

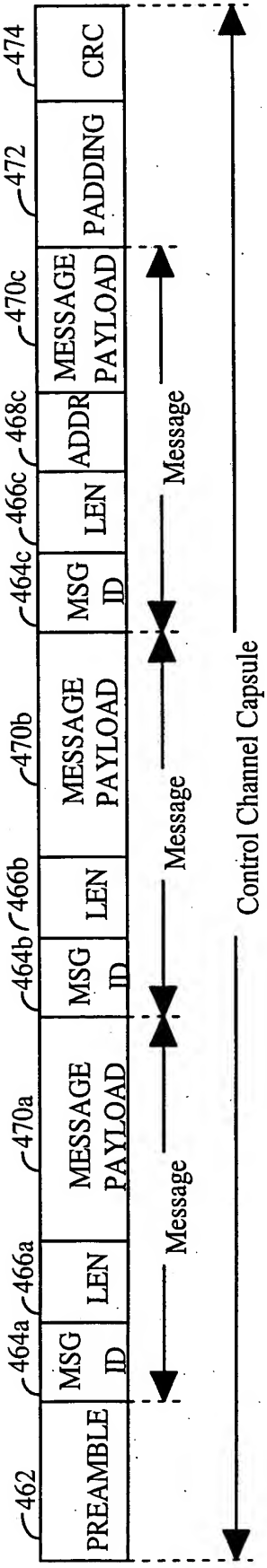

FIG. 4G

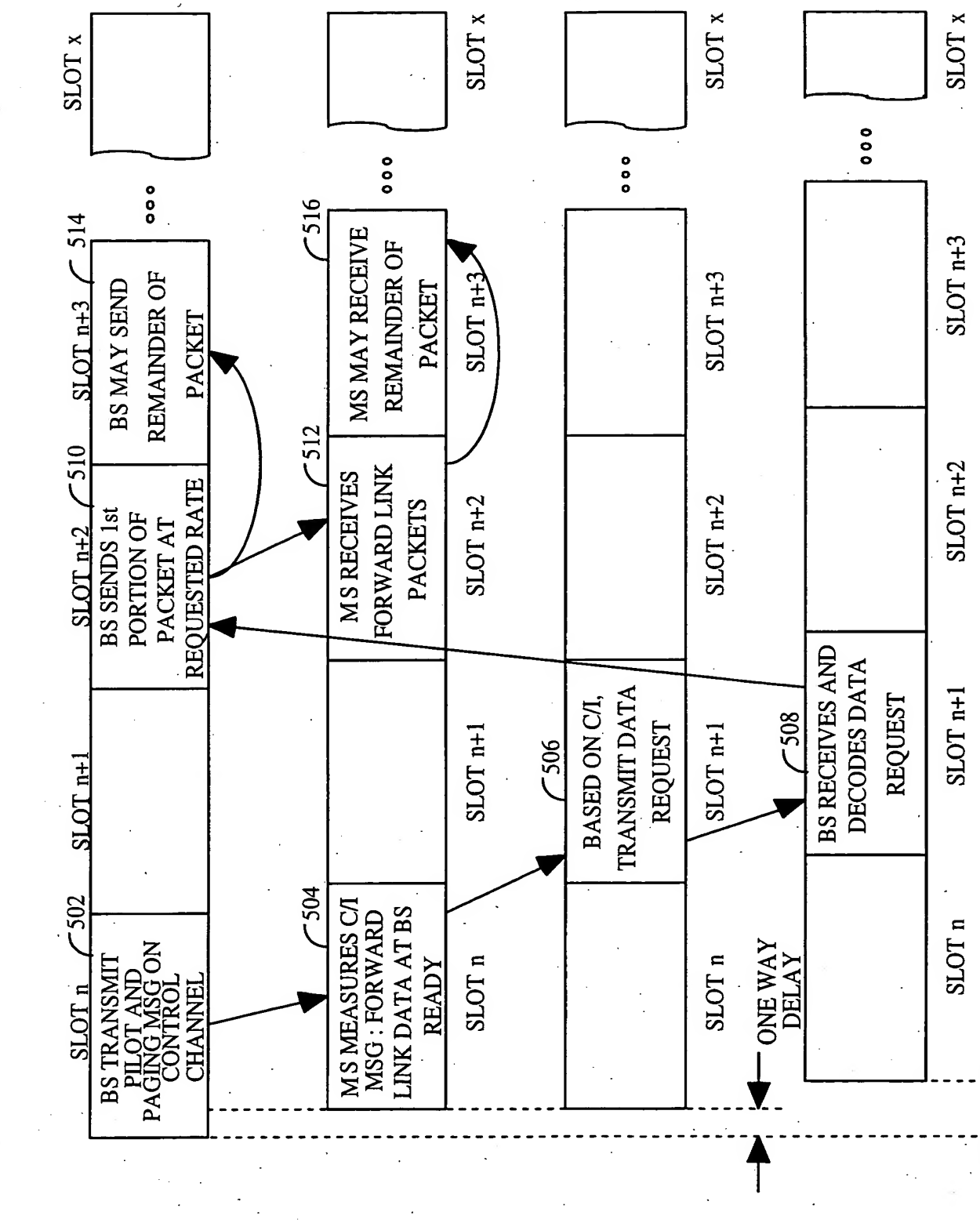
BASE STATION TRANSMIT
MOBILE STATION RECEIVE
MOBILE STATION TRANSMIT
BASE STATION RECEIVE
SLOT n
SLOT n+1
SLOT n+2
SLOT n+3
SLOT x
502
504
506
508
510
512
514
516
BS TRANSMIT PILOT AND PAGING MSG ON CONTROL CHANNEL
MS MEASURES C/I MSG : FORWARD LINK DATA AT BS READY
BASED ON C/I, TRANSMIT DATA REQUEST
BS RECEIVES AND DECODES DATA REQUEST
BS SENDS 1st PORTION OF PACKET AT REQUESTED RATE
MS RECEIVES FORWARD LINK PACKETS
BS MAY SEND REMAINDER OF PACKET
MS MAY RECEIVE REMAINDER OF PACKET
ONE WAY DELAY
ROUND TRIP DELAY

FIG. 5

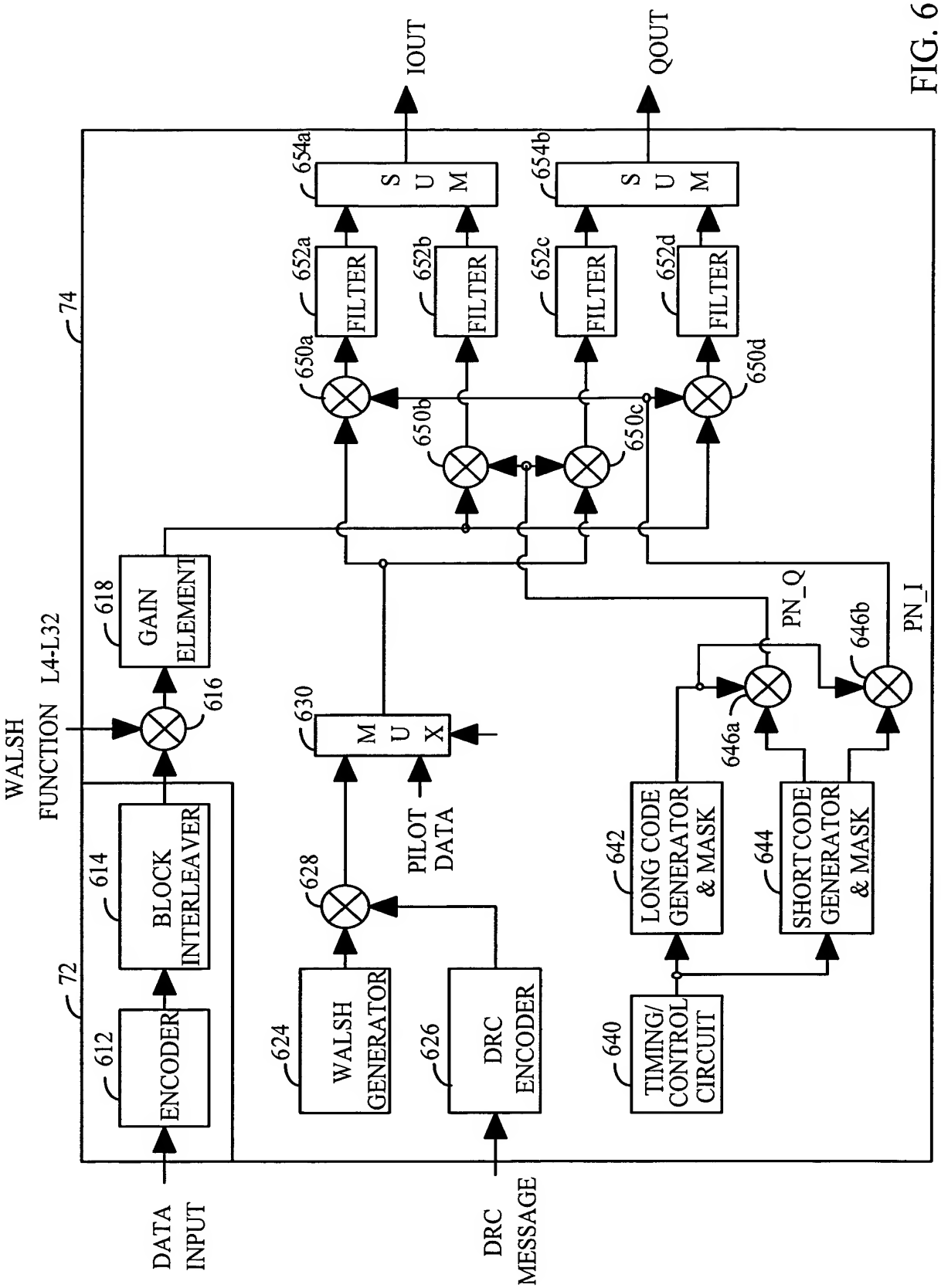
IOUT
QOUT
654a
654b
SUM
652a
652b
652c
652d
FILTER
650a
650b
650c
650d
74
618
GAIN ELEMENT
WALSH FUNCTION L4-L32
616
630
MUX
PN_Q
PN_I
646b
646a
614
BLOCK INTERLEAVER
628
PILOT DATA
642
LONG CODE GENERATOR & MASK
644
SHORT CODE GENERATOR & MASK
72
612
ENCODER
624
WALSH GENERATOR
626
DRC ENCODER
640
TIMING/ CONTROL CIRCUIT
DATA INPUT
DRC MESSAGE

FIG. 6

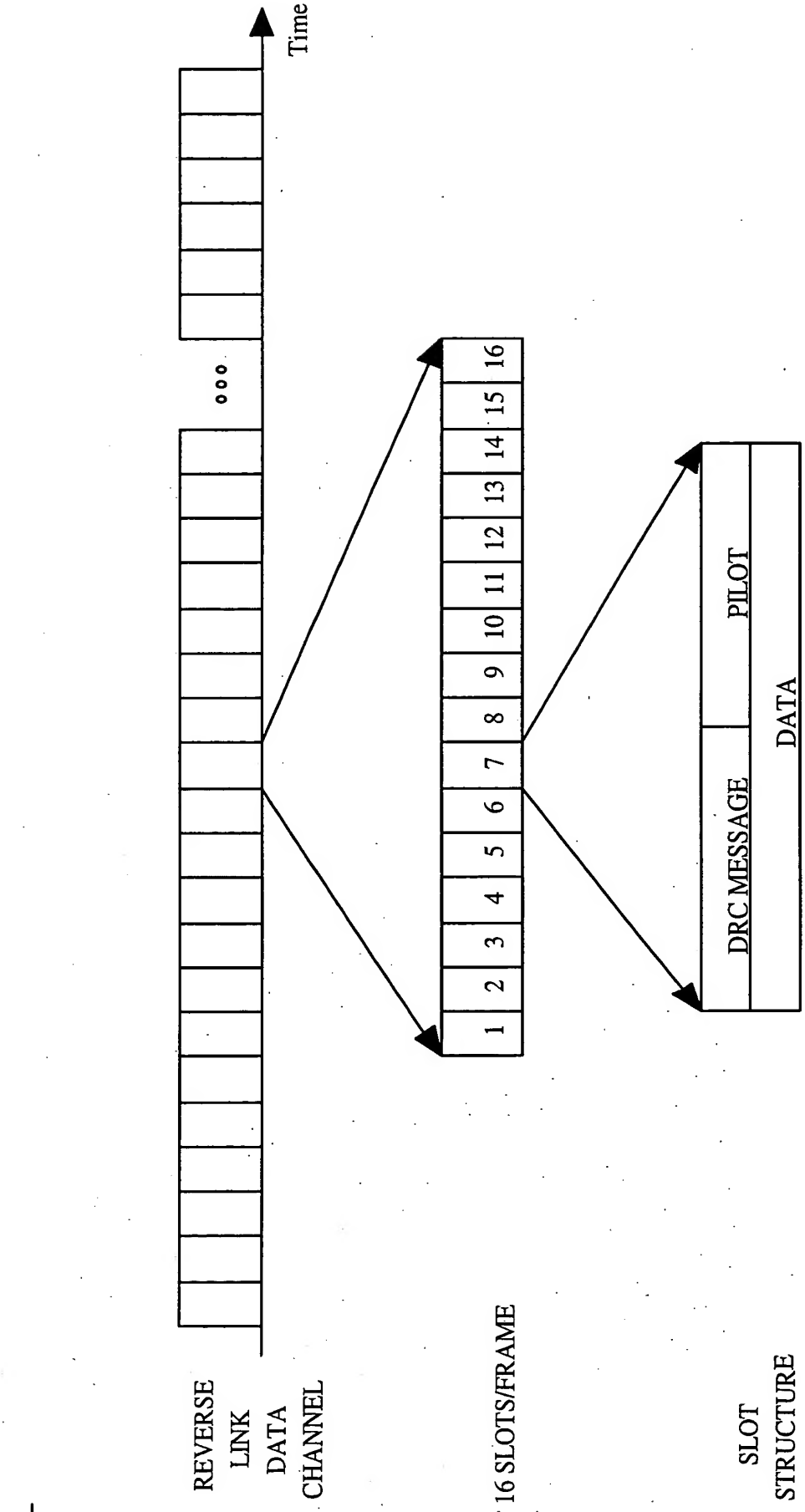
Time
REVERSE LINK DATA CHANNEL
16 SLOTS/FRAME
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
SLOT STRUCTURE
DRC MESSAGE
PILOT
DATA

FIG. 7A

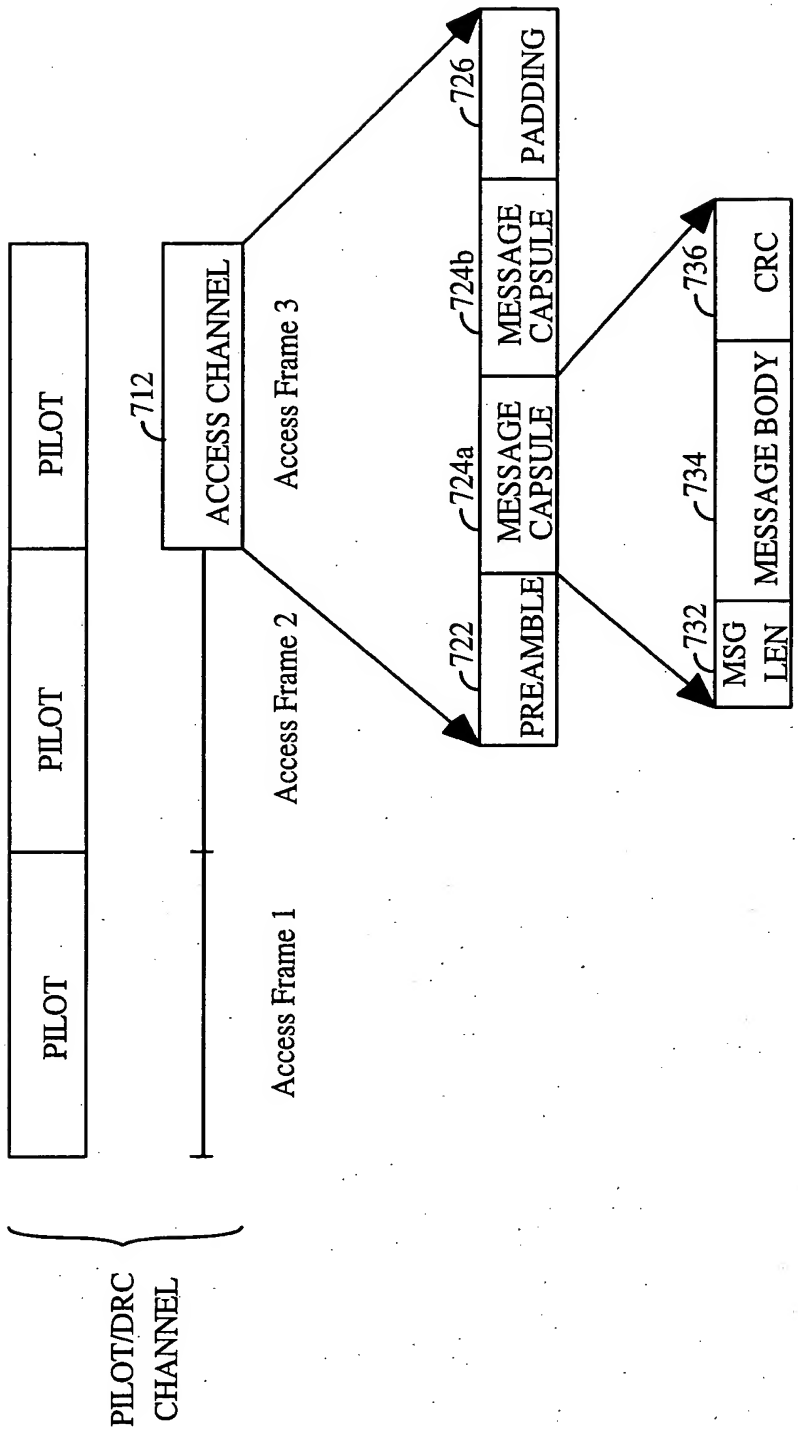
PILOT
PILOT
PILOT
PILOT/DRC CHANNEL
712
ACCESS CHANNEL
Access Frame 1
Access Frame 2
Access Frame 3
722
PREAMBLE
724a
MESSAGE CAPSULE
724b
MESSAGE CAPSULE
726
PADDING
732
MSG LEN
734
MESSAGE BODY
736
CRC

FIG. 7B

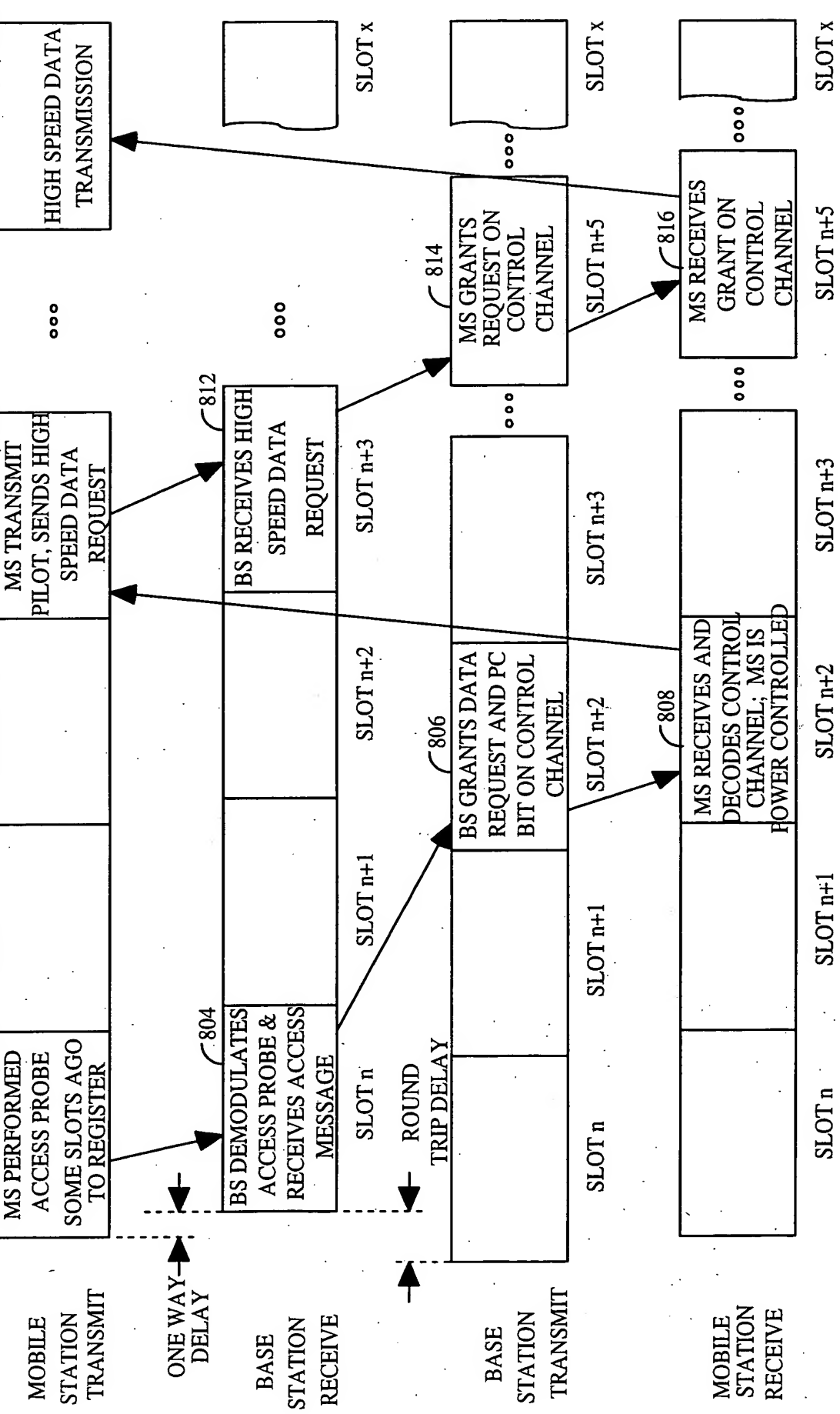
MOBILE STATION TRANSMIT
ONE WAY DELAY
BASE STATION RECEIVE
ROUND TRIP DELAY
BASE STATION TRANSMIT
MOBILE STATION RECEIVE
SLOT n
SLOT n+1
SLOT n+2
SLOT n+3
SLOT n+5
SLOT n+6
SLOT x
MS PERFORMED ACCESS PROBE SOME SLOTS AGO TO REGISTER
802
BS DEMODULATES ACCESS PROBE & RECEIVES ACCESS MESSAGE
804
BS GRANTS DATA REQUEST AND PC BIT ON CONTROL CHANNEL
806
MS RECEIVES AND DECODES CONTROL CHANNEL; MS IS POWER CONTROLLED
808
MS TRANSMIT PILOT, SENDS HIGH SPEED DATA REQUEST
810
BS RECEIVES HIGH SPEED DATA REQUEST
812
MS GRANTS REQUEST ON CONTROL CHANNEL
814
MS RECEIVES GRANT ON CONTROL CHANNEL
816
HIGH SPEED DATA TRANSMISSION
818

FIG. 8

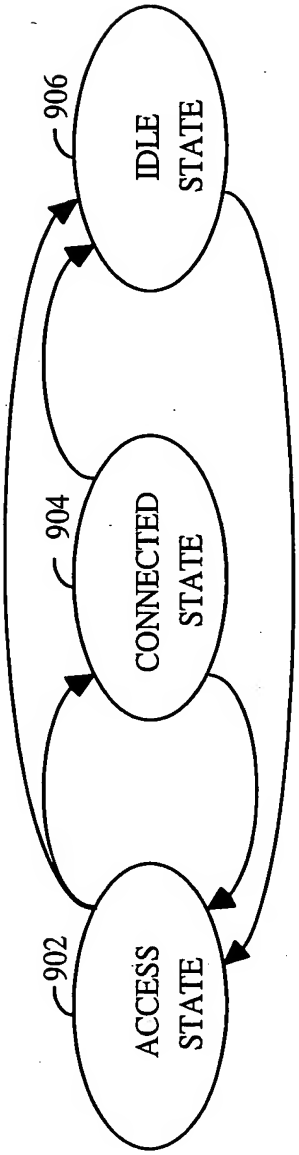

FIG. 9

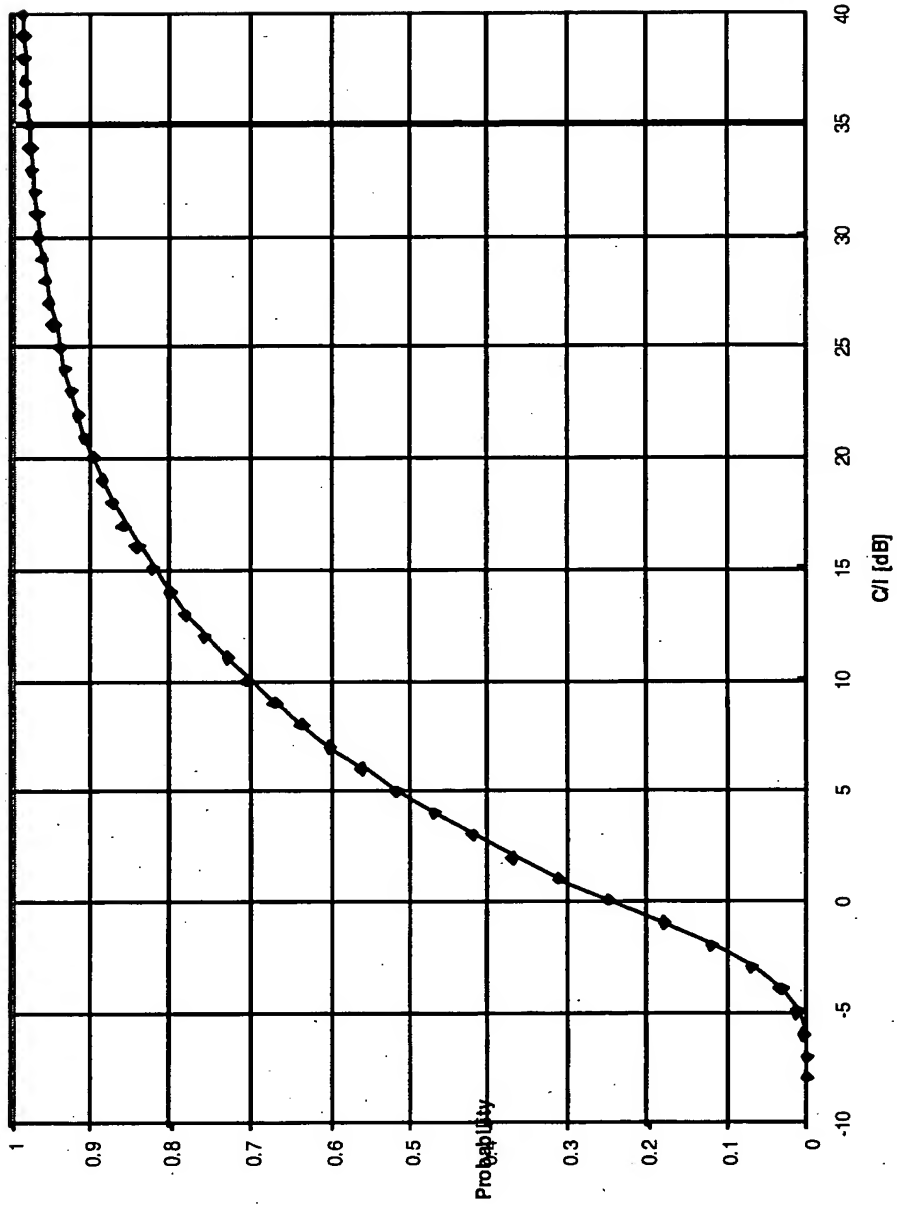
1
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
Probability
40
35
30
25
20
15
10
5
0
-5
-10
C/I [dB]

FIG. 10